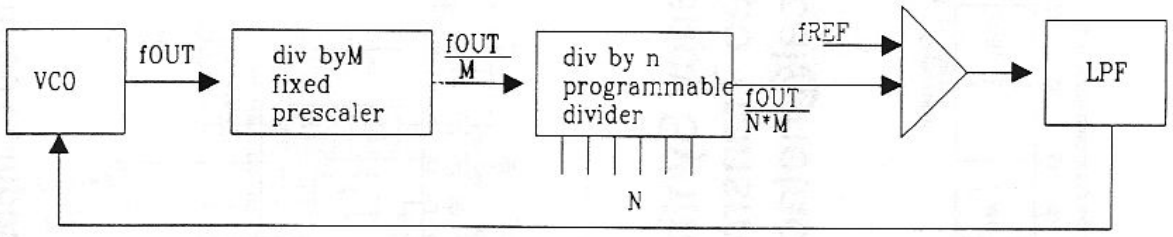
PLL Design

This is a preliminary design for a digitally synthesized fm stereo transmitter using the BA1404. MC145151-1(pll synthesizer) and the MC12019(div by 10/11 prescailer).



fIN = fREF

$fIN = \frac{fOUT}{N*M}$

fOUT = (N*M)fREF

fOUT = N(M*fREF) -> fSTEP = M * fREF

We Want:

fSTEP = 100khz

fOUT = 87.5 -108.1mhz

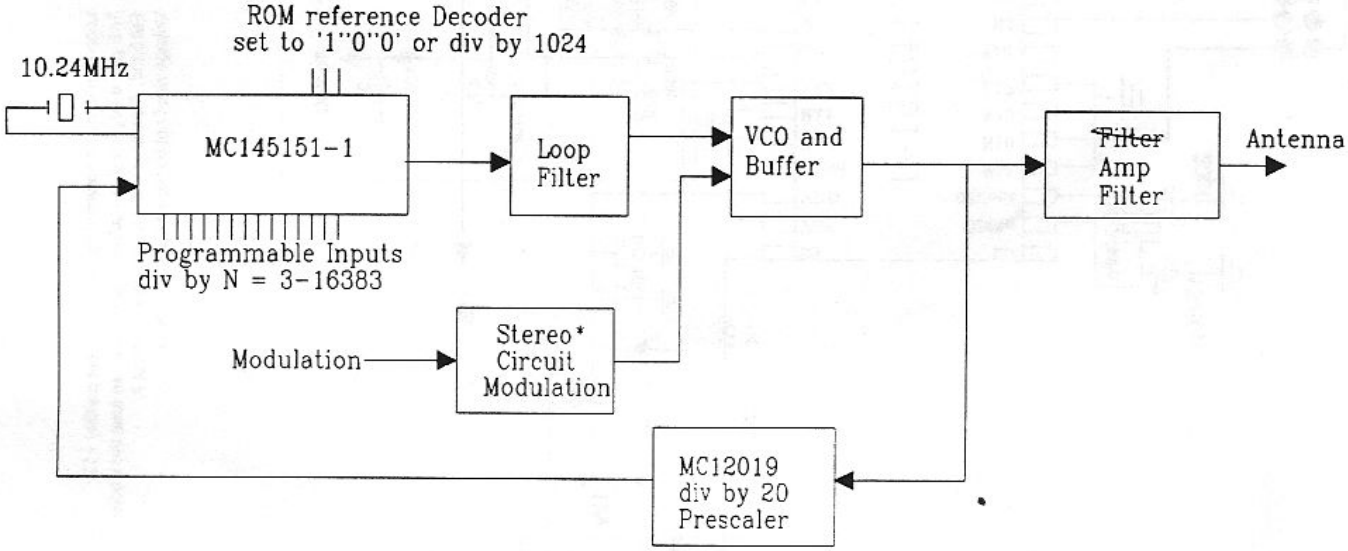
M = 20 --> MC12019

N = 3 - 16383 --->MC145151-1

$fREF = \frac{fSTEP}{M} = 5khz$

(5khz * 1024)*2 = 10.24 mhz Ref Osc. for MC145151-1
using 100 for the reference address divide value

$N = \frac{fOUT(mhz)}{.1}$ ⟶ so 87.5mhz ---> n=875, 108.1mhz ---> n=1081... totally cool



* Stereo Modulation Circuit - See notes under car CD player

o We are only interested in N=877 to 1081 we can limit the inputs to this range or be carful not to go out of these bounds.

o I am having trouble finding examples on how to modulate the VCO. most PLL books have this block diagram but give no circuit examples.

o The filter-amp-filter section will be close to simple 3 element filter from the FM-10 FAQ. an amp close to the dual 901 amp. and another 3 element filter. I am hoping for between 100mw-500mw. depending on the output from the VCO.

o Please see National Semiconductor "Interface Databook" 1990 for further info on PLL design. including schematics for VCO.

o Contact me for further info/spec sheets etc if you ars project or have any ideas or examples for the above.